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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,300	12/28/2001	Hong Suk Yoo	8733.508.00-US	2980

30827 7590 10/01/2003
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EXAMINER

DUONG, THOI V

ART UNIT PAPER NUMBER

2871

DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/028,300

Applicant(s)

YOO ET AL.

Examiner

Thoi V Duong

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 ~~is/are~~ pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5,6 and 17-31 ~~is/are~~ allowed.
- 6) ☒ Claim(s) 1-4 and 7-16 ~~is/are~~ rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the RCE, Paper No. 12, filed July 15, 2003.

Accordingly, claims 1 and 7 are amended. Currently, claims 1-31 are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-4 and 7-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawahata (USPN 6,356,318 B1).

As shown in Figs. 1 and 2, Kawahata discloses a liquid crystal display (LCD) device comprising:

a gate line 7 (and 7') and a data line 13 on a substrate 1 to cross each other;

a thin film transistor 11 including a gate electrode 7a, a source electrode 13a, and a drain electrode 14,

and provided at an intersection between the data line and the gate line,

wherein the gate electrode is connected to the gate line,

wherein the source electrode is connected to the data line,

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wherein the drain electrode is opposed to the source electrode, and
wherein a channel is formed between the source electrode and the drain electrode;

a storage electrode 15 directly on and at the interior of a gate insulating film 10 (col. 4, lines 46-48) to overlap with the gate line,

wherein the gate insulating film formed on the substrate to cover the gate electrode and to entirely overlap with the gate line and to electrically isolate the gate line and the data line from each other,

wherein the storage capacitor includes the storage electrode 15 and the gate line 7' opposed to each other and having the gate insulating film formed therebetween;

wherein a distance between the gate line and the storage electrode is in the range of 500 to 1500 Å (col. 4, lines 38-39);

an active layer 12 formed on the gate insulating film to overlap with the gate electrode; and

a protective layer 16 formed on the gate insulating film to cover the gate line, the data line, and the thin film transistor,

wherein a transparent pixel electrode 19 (col. 5, lines 50-53) is connected to the drain electrode via a first contact hole 17 provided on the protective layer,

wherein the storage electrode is connected to the transparent pixel electrode 19 via a second contact hole 18 provided on the protective layer,

Finally, with respect to claim 9, although an ohmic contact layer is not shown, it is well-known for forming an ohmic contact layer on the active layer 12 in a TFT fabrication.

R s p n s e t o A r g u m e n t s

4. Applicant's arguments filed July 15, 2003 have been fully considered but they are not persuasive.

With respect to claims 1 and 7, Applicant argued that the reference of Kawahata does not teach a storage electrode directly on and at the interior of a gate insulating film to overlap with the gate line as recited in claim 1 or a storage electrode directly on and at the interior of a gate insulating film which is entirely overlapping with the gate line as recited in claim 7. The Examiner disagrees with the Applicant's remarks since, as clearly shown in Fig. 1, the storage electrode 15 is formed directly on and at the interior of the insulating film 10 which is also a gate insulating film in addition to the gate insulating film 8 (col. 4, lines 46-48). This storage electrode 15 overlaps with the gate line 7' and the gate insulating film 10 is entirely overlapping with the gate line 7'.

Allowable Subject Matter

5. Claims 5, 6 and 17-31 were previously allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 5 and 17, none of the prior art of record discloses, in combination with other limitations as claimed, a storage electrode formed on a first gate insulating film to overlap with the gate line, a second gate insulating film deposited on the first gate insulating film to cover the storage electrode, and an active layer and an ohmic contact layer formed on the gate insulating films.

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The most revelant reference, USPN 6,356,318 B1 of Kawahata, fails to disclose or suggest a second gate insulating layer formed on top of the storage electrode. The Kawahata's reference only discloses the storage electrode formed on top of and inside the concave portion on the second gate insulating layer as shown in Fig. 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong



09/25/2003



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